BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

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File Number: T 889/90 - 3.5.1

Application No.: 84 111 589.2

Publication No.: 139 254

Title of invention: Apparatus and method for direct memory to peripheral and peripheral to memory data transfer

Classification: G06F 13/28

D E C I S I O N
of 19 June 1991

Applicant: International Business Machines Corporation

Headword:

EPC Article 56

Keyword: "Inventive step (no)"

Headnote

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 889/90 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 19 June 1991

Appellant : International Business Machines Corporation
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Representative : Rudolph, Wolfgang
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Decision under appeal : Decision of Examining Division 065 of the European Patent Office dated 1 June 1990 refusing European patent application No. 84 111 589.2 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : A.S. Clelland
C. Holtz

Summary of Facts and Submissions

I. Appellant's European patent application No. 84 111 589.2, filed on 28 September 1984, claiming priority of a previous application in the United States dated 18 October 1983, was refused by a decision of the Examining Division dated 1 June 1990. The decision was based on Claims 1 to 4 as filed with a letter dated 7 March 1990, received on 12 March 1990.

II. The reason given for the refusal was that the subject-matter of Claim 1 lacked an inventive step having regard to the prior art known from the following document:

D1: WESCON Conference Record, Volume 25, September 1981, Paper 3/1, pages 1 to 7, EL SEGUNDO, US. HASTINGS et al: "Minimum chip-count number cruncher uses bipolar co-processor".

III. On 27 July 1990 the Appellant filed a notice of appeal, together with the appeal fee, and requested cancellation of the decision. A statement setting out the grounds of appeal was subsequently filed on 28 September 1990.

IV. In a communication pursuant to Article 110(2) EPC, the Board raised the question of whether Claim 1 complied with Article 84 EPC as to clarity. This objection had not been raised by the Examining Division in the impugned decision. The Board moreover expressed the provisional opinion that the subject-matter of Claim 1, insofar as the claim could be understood, did not involve an inventive step having regard to the disclosure of D1.

V. In response to the communication the Appellant, in a letter received on 3 May 1991, maintained the claims unamended and argued that Claim 1 was clear and inventive.

VI. The Appellant requests that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims

Claims 1 to 4 received on 12.03.90.

Description

Pages 4 to 13 as originally filed.
Pages 1, 1a, 2, 2a, 3, 3a received on 12.03.90.

Drawings

Sheets 1 to 4 as originally filed.

VII. Claim 1 reads as follows:

"Apparatus for effecting data transfer to and from a selected one of a plurality of memory mapped peripheral devices in a microprocessor implemented data processing system (10) having main storage means (24), control storage means (26) with a plurality of locations (30) in said control storage means (26), each having a unique address associated therewith, one each of said locations being mapped to a different one of the plurality of peripheral devices (16), a system bus (18, 22) connecting the microprocessor (12, 14), peripheral devices (16) and the storage, having further first control logic means (40, 42, 44, 50, 54), connected between said plurality of

peripheral devices and said plurality of memory mapped control storage locations, for detecting an access to any one of said memory mapped locations and for generating an initiate peripheral operation signal (46) in response thereto that will ready said peripheral (16) for operation upon receipt thereof, characterized

by second control logic means (62, 68, 78, 86, 96, 108, 118, 130), associated with said microprocessor, for placing a peripheral (16) authorizing signal (80, 120) in one cycle of the system bus on the output thereof whenever said microprocessor (12) does a memory (24) access on behalf of a readied peripheral; and

by third control logic means (90, 92, 124), connected to and between said microprocessor, said accessed peripheral device and said system bus, for granting system bus control to a readied peripheral in response to an authorizing signal (120) therefor,

by buffering means (90, 92) having bidirectional data flow and a switchable input (124) which controls the direction of data flow therethrough, connected between said peripherals (16) and said system bus (22), for switching the direction of data flow to and from an accessed peripheral in accordance with a signal applied to said switchable input thereof."

VIII. The Appellant's arguments in support of an inventive step can be summarised as follows:

Although D1 discloses apparatus for effecting data transfer as set forth in the preamble of Claim 1, it does not disclose the use of second control logic means for placing a peripheral authorising signal in one cycle of the system bus whenever the microprocessor does a memory

access on behalf of a readied peripheral unit, nor does it disclose the provision of third control means or buffering means which grant system bus control to a readied peripheral unit in response to an authorising signal generated by the second control logic means, the direction of data flow being switchable in accordance with a signal applied to the buffering means. The main processor can thereby access a cache system for a single piece of data every clock period whilst simultaneously the cache system continues to accept data being brought in from the memory system.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. The amendments made to the application documents do not contravene Article 123(2) EPC and are, therefore, also admissible.

3. Clarity

3.1 Before considering whether Claim 1 complies with Article 52(1) EPC it is necessary to address the issue of the clarity of the claim. In its communication the Board essentially raised the following three points:

(a) No clear distinction appears to exist between the "initiate peripheral operation" and "peripheral authorising" signals of the first and second control logic means respectively, or between them and the operation of the third control logic means in "granting system bus control to a readied peripheral".

(b) The limitative effect of the second control logic means placing the peripheral authorising signal "in one cycle of the system bus on the output thereof" is not clear. It is, moreover, not clear on the output of what the signal is placed.

(c) The buffering means, although claimed as a separate feature, appear from the description to form part of the third control logic means.

3.2 The Appellant's response to these objections is largely an assertion that Claim 1 is clear. The Appellant further asserts that the signals generated by the respective control logic means are "logically connected together" but are clearly different signals. He then goes on to discuss the operation of the claimed apparatus in terms which are not easy to relate to the invention either as claimed or described. Reference is made to sending a command to the selected peripheral unit when peripheral operation is desired, together with initiation of a memory fetch or store cycle. The address of the needed data is said to be provided on the address bus, together with a "special decode that indicates the unique nature of this memory access". On detection of this special decode the data bus is intercepted, presumably by the peripheral, at the appropriate point in the bus cycle. The correct control signals are thereupon applied to the peripheral unit to enable the desired data transfer.

3.3 It is not clear to the Board what the Appellant means by a "special decode that indicates the unique nature of this memory access"; the claim makes no reference to any "special decode" and the Board can only conclude that the signal being referred to is the special memory access signal (72) which indicates a system/370 memory access and

which is specifically referred to at features (e) and (f) of Claim 4. Such a signal is not an explicit feature of Claim 1.

3.4 The Board has, however, been able to interpret Claim 1 by reference to the description (Article 69(1) EPC). From the description it appears that the first logic means of the claim serve to decode the relevant memory-mapped address and to condition the peripheral to accept either a command or data, see page 8, line 29 to page 10, line 4.

3.5 At page 10, lines 5 and 6 it is stated that once the peripheral has been conditioned to accept a command, "the next step is to advise the peripheral of the nature of the command". From lines 6 to 13 of the same page it is clear that by "nature of the command" is meant whether the peripheral is to perform a memory read or a memory write. In this connection, lines 26 to 28 of page 10 and lines 2 to 6 of page 11 refer to setting the write command pin 82 of the peripheral so as to condition it to accept the data it will need to perform its floating point function. When manipulated data is to be transferred from the peripheral to memory the peripheral is firstly advised it should accept a command by appropriately setting its input pin 48 (i.e. the COMMAND/DATA pin) and then the primary processor initiates a peripheral read operation by setting a read enable output, see page 11, line 26 to page 12, line 20.

3.6 It therefore appears to the Board that the peripheral authorising signal of the second control logic means must be interpreted as serving to condition the peripheral to a read or a write mode.

3.7 The reference to the second control logic means placing the peripheral authorising signal "in one cycle of the system bus on the output thereof" must be interpreted, in

the light of the description, as referring to placing the peripheral authorising signal on the output of the second control logic means during one cycle of the system bus. It may be that the claim was intended by the Appellant to cover some aspect of a peripheral-to-memory read or write operation taking place within a single system bus cycle, but this is not what the claim states; the Appellant has chosen not to comment on the question of interpretation raised by the Board in its communication.

3.8 The third control logic means are understood as including the buffering means which when enabled permit the peripheral to read to or write from main memory, see page 12, lines 10 to 20 of the description. By control of the buffering means, system bus control is effectively granted to the peripheral.

4. **Novelty**

4.1 The Board agrees with the Appellant that the single most relevant prior art document is D1. The apparatus known from D1 effects data transfer to and from a selected one of a plurality of memory mapped peripheral devices in a microprocessor implemented data processing system, see Figure 1, in which a bipolar co-processor and "peripherals" are shown. Main storage means are present as in any microprocessor system and these storage means include locations serving as control storage means each having a unique address associated therewith, each of said locations being mapped to a different peripheral device. These features are standard practice in the art, as is the provision of a system bus connecting the microprocessor, peripheral devices and the memory.

4.2 In D1 at page 1, left hand column, heading "Co-processor operation" it is stated that a co-processor "...

recognises instructions and data intended for itself. This arrangement is much faster than routing all data and commands through the host. Information is picked off the system bus directly." This is in effect saying that the system can be speeded up by granting direct access of the co-processor to the memory. According to the same page, right hand column, lines 2 to 6, a command to the appropriate address activates the co-processor and sets it up for "the operations and data formats to be handled". According to lines 6 to 9, the co-processor recognises "specified host instructions and retrieves its input data from the bus". The data from the bus must originate in main memory. At lines 16 to 18 a programmable array logic (PAL) device is described which serves "to decode the selected host 'fetch' instruction".

4.3 The mode of operation described above and the presence of the PAL device would be understood by the skilled man to refer to control logic means monitoring the relevant memory locations and serving firstly to detect a call on the co-processor, thereafter to distinguish between instructions and data, in the event of a data operation to set up the co-processor for either a data read or a data write operation and finally to pass control to the co-processor. These are the functions understood by the Board to be carried out by the first, second and (part of the) third control logic means, which are accordingly present in the D1 apparatus.

No mention is made in D1 of buffering means. Claim 1 is accordingly novel with respect to D1.

5. **Inventive Step**

5.1 It is general practice to buffer devices connected to the system bus and in a case such as a co-processor as

disclosed in D1, in which data is fed to the co-processor and then, after completion of the calculations, read back into memory, such buffering must be bidirectional. This necessitates the system hardware recognising when the peripheral is reading data from, or writing data to, the memory and switching the buffer accordingly. The skilled man would find it obvious to provide such buffering in conjunction with the D1 arrangement.

5.2 The Board has accordingly come to the conclusion that the skilled person, implementing the teaching of document D1, would arrive in an obvious manner at apparatus having all the features specified in Claim 1. The subject-matter of Claim 1 does not, therefore, involve an inventive step.

6. The arguments submitted by the Appellant in support of an inventive step are not convincing.

6.1 In the statement of grounds, other than assertions that the second and third control logic means are not present in D1, the Appellant states:

> "The significant feature of the invention is to allow the processor to access the cache system for a single piece of data every clock period while simultaneously the cache system continues to accept data being [brought] in from the memory system. Only a single set of address translation and cache tag (directory) hardware is required and, furthermore, only a single-port cache array is required, resulting in significantly less circuitry than the prior art."

The Board is unable to relate this statement to any of the subject-matter of the application. Nowhere does the application refer to a cache system, the peripheral of the described embodiment being a floating point processor

apparently of the same kind as in D1. The response to the Board's communication merely repeats the arguments brought forward in the statement of grounds.

7. The Board, therefore, concludes that the subject-matter of Claim 1 lacks an inventive step (Article 56 EPC) and the claim, therefore, fails to comply with Article 52(1) EPC.

8. Claims 2 to 4 must share the fate of Claim 1. Furthermore, they do not appear to include any feature which could involve an inventive step.

9. Finally, even if Claim 1 had as apparently intended been limited to peripheral operation in a single bus cycle, the claim would still have been found to lack an inventive step. The object of the invention is given in the originally filed application at page 3 as being (firstly) the transfer of data between main memory and a peripheral device in only one bus cycle of the main processor, whilst (secondly) avoiding the need to route data through the internal storage area of the main processor during any such transfer.

Any arrangement which achieves the latter object will as a matter of course also achieve the former. Clearly, in D1 direct memory access is granted to the peripheral without intermediate storage. Direct data transfer - as disclosed in D1 - thus implies transfer in a single bus cycle.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg