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**Datasheet for the decision of 13 September 2024**

**Case Number:** T 2436/22 - 3.5.05

**Application Number:** 15202883.3

**Publication Number:** 3188025

**IPC:** G06F12/08

**Language of the proceedings:** EN

**Title of invention:**
Memory node with cache for emulated shared memory computers

**Applicant:**
Teknologian tutkimuskeskus VTT Oy

**Headword:**
Separate data memory node/TUTKIMUSKESKUS

**Relevant legal provisions:**
EPC Art. 123(2)
RPBA 2020 Art. 12(4), 12(6), 13(2)

**Keyword:**

Added subject-matter - main, 1st and 2nd auxiliary requests (yes)
Admittance of claim amendments filed on appeal - 3rd auxiliary request (no): "fresh case" + should have been submitted in the examination proceedings
Admittance of claim amendments filed after notification of Art. 15(1) RPBA communication - 4th and 5th auxiliary requests (no): no "exceptional circumstances" + no *prima facie* allowability

**Decisions cited:**

G 0001/93, G 0002/10, T 0089/00, T 2271/18, T 2632/18

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**Case Number: T 2436/22 - 3.5.05**

# D E C I S I O N
# of Technical Board of Appeal 3.5.05
# of 13 September 2024

| | |
|---|---|
| **Appellant:** (Applicant) | Teknologian tutkimuskeskus VTT Oy<br>Vuorimiehenkatu 3 (Espoo)<br>02044 VTT (FI) |
| **Representative:** | Aaltonen, Janne Lari Antero<br>Moosedog Oy<br>Vähäheikkiläntie 56 C<br>20810 Turku (FI) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 1 June 2022 refusing European patent application No. 15202883.3 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

| | |
|---|---|
| **Chair** | K. Bengi-Akyürek |
| **Members:** | N. H. Uhlmann |
| | F. Bostedt |

## Summary of Facts and Submissions

I. The appellant appealed against the examining division's decision to refuse the present European patent application. The examining division held that:

- the main request and the first auxiliary request did not comply with Article 123(2) EPC;

- the second auxiliary requests did not comply with Article 56 EPC.

II. Oral proceedings before the board took place on 13 September 2024. At the end of them, the board's decision was announced.

The appellant requested that the decision under appeal be set aside and that a patent be granted according to the **main request**, or as an alternative, according to one of the **first to third auxiliary requests** (filed with the statement setting out the grounds of appeal) or the **fourth and fifth auxiliary request** (filed during the oral proceedings before the board).

III. Claim 1 of the **main request** reads as follows:

"A parallel processor system, comprising a plurality of processors (102), multiple, physically distributed data memory nodes (400) that are logically shared between the processors, and an interconnection network (108) connecting the plurality of processors and said multiple data memory nodes for use in ESM (Emulated Shared Memory) architectures (100, 200), **characterized in that** each one of the data memory

nodes (400) is separate with respect to related hardware of the processors (102), and wherein each shared data memory node comprises:

a data memory module (402) containing data memory for storing input data therein and retrieving stored data therefrom responsive to predetermined control signals,

a multi-port cache (404) for the data memory, said cache being provided with at least one read port (404A, 404B) and at least one write port (404C, 404D, 404E), said cache (404) being configured to hold recently and/or frequently used data stored in the data memory (402), and

an active memory unit (406) at least functionally connected to a plurality of processors via said interconnection network (108), said active memory unit (406) being configured to operate the cache (404) upon receiving a multioperation reference (410) incorporating a memory reference to the data memory of the data memory module from a number of processors of said plurality,

wherein responsive to the receipt of the multioperation reference the active memory unit (406) is configured to process the multioperation reference according to the type of the multioperation indicated in the reference and execute inter-processor portion of the multioperation, utilizing cached data in accordance with the memory reference and data provided in the multioperation reference."

IV. Claim 1 of the **first auxiliary request** differs from claim 1 of the main request in that the first clause of the characterising portion reads:

> "each one of the data memory nodes (400) is separate with respect to related hardware of the processors (102), wherein the related hardware comprise step caches and scratchpads associated with the processors."

V. Claim 1 of the **second auxiliary request** differs from claim 1 of the main request in that

- the wording "each associated with" has been added after "a plurality of processors (102),";

- the following wording has been deleted "each one of the data memory nodes (400) is separate with respect to related hardware of the processors (102)" and

- the wording "an active memory unit (406) at least functionally connected to a plurality of processors via said interconnection network (108)" has been replaced by the phrase "an active memory unit (406) at least functionally connected to a plurality of processors, said step caches, and said scratchpads via said interconnection network (108)".

VI. Claim 1 of the **third auxiliary request** reads as follows:

"A parallel processor system, comprising a plurality of processors (102) and processor-associated hardware including step caches, scratchpads, and buffers; and multiple, physically distributed data memory nodes (400) that are logically shared between the processors, and an interconnection network (108) connecting the plurality of processors and processor-associated hardware, and said multiple data memory nodes for use in ESM (Emulated Shared Memory) architectures (100, 200), **characterized in that** each shared data memory node comprises:

a data memory module (402) containing data memory for storing input data therein and retrieving stored data therefrom responsive to predetermined control signals,

a multi-port cache (404) connected to the data memory module (402), said multiport cache being provided with at least one read port (404A, 404B) and at least one write port (404C, 404D, 404E), said multi-port cache (404) being configured to hold recently and/or frequently used data stored in the data memory (402), and

an active memory unit (406) at least functionally connected to the plurality of processors and processor-associated hardware via said interconnection network (108), said active memory unit (406) being connected and configured to operate the multi-port cache (404) upon receiving, via said interconnection network (108), a multi operation reference (410) incorporating a memory reference to the data memory of

the data memory module (402) from a number of processors of said plurality,

wherein responsive to the receipt of the multioperation reference (410) the active memory unit (406) is configured to process the multioperation reference according to the type of the multioperation indicated in the multioperation reference (410) and execute inter-processor portion of the multioperation, utilizing cached data in the multi-port cache (404) in accordance with the memory reference and data provided in the multioperation reference (410), and wherein the data memory node (400) is configured to return the outcome of the executed multioperation to said number of processors via said interconnection network (108)."

VII. Claim 1 of the **fourth auxiliary request** differs from claim 1 of the main request in that the wording "each one of the data memory nodes (400) is separate with respect to related hardware of the processors (102)" has been replaced by the phrase

"each one of the data memory nodes (400) is functionally separate with respect to related hardware of the processors (102)".

VIII. Claim 1 of the **fifth auxiliary request** differs from claim 1 of the second auxiliary request in that

- the wording "step caches, and scratchpads" has been added after "a plurality of processors (102)," and

- the wording "an active memory unit (406) at least functionally connected to plurality of processors,

said step caches and said scratchpads" has been replaced by

"an active memory unit (406) at least functionally connected to the plurality of processors, including their associated step caches and scratchpads".

## Reasons for the Decision

1. The present application pertains to a system including multiple processors, multiple, physically distributed shared "data memory nodes" and an interconnection network connecting them. The data memory nodes comprise "data memory modules" which store data, a "multi-port cache" and an "active memory unit" which operates the multi-port cache and processes multi-operations received from the processors.

2. **Main request and first auxiliary request - claim 1 - Article 123(2) EPC**

**2.1** The **main request** is identical to the main request underlying the contested decision. Claim 1 of the main request includes the following limiting features (board's labelling and emphasis):

(a) A parallel processor system, comprising
(b) a plurality of processors,
(c) multiple, physically distributed data memory nodes that are logically shared between the processors, and
(d) an interconnection network connecting the plurality of processors and said multiple data memory nodes

for use in ESM (Emulated Shared Memory) architectures, wherein

(e) each one of the data memory nodes is separate with respect to related hardware of the processors, and

(f) wherein each shared data memory node comprises:

(g) a data memory module containing data memory for storing input data therein and retrieving stored data therefrom responsive to predetermined control signals,

(h) a multi-port cache for the data memory, said cache being provided with at least one read port and at least one write port, said cache being configured to hold recently and/or frequently used data stored in the data memory, and

(i) an active memory unit at least functionally connected to a plurality of processors via said interconnection network,

(j) said active memory unit being configured to operate the cache upon receiving a multi-operation reference incorporating a memory reference to the data memory of the data memory module from a number of processors of said plurality,

(k) wherein responsive to the receipt of the multi-operation reference the active memory unit is configured to process the multi-operation reference according to the type of the multi-operation indicated in the reference and execute inter-processor portion of the multi-operation, utilising cached data in accordance with the memory reference and data provided in the multi-operation reference.

2.2 Feature (e) of claim 1 of the main request was modified in claim 1 of the **first auxiliary request** as follows:

(e1) each one of the data memory nodes is separate with respect to related hardware of the processors, wherein the related hardware comprise step caches and scratchpads associated with the processors.

2.3 The board endorses the finding in the impugned decision that **feature (e)** does not comply with Article 123(2) EPC.

2.4 To begin with, the board notes that the expression "is separate with respect to" (cf. feature (e)) is quite broad and not further defined. A skilled reader would consider that both a functional separation and different types of hardware separation (e.g. *separate* integrated circuits and *separate* areas on one chip) are encompassed by the scope of claim 1. To comply with Article 123(2) EPC, a basis for at least these technically meaningful interpretations is needed.

2.5 The appellant argued that it was important to define the skilled reader and its knowledge. In particular, a hardware engineer and a software engineer possessed different skills and would interpret both claim 1 and the teaching of the application as filed differently. Furthermore, the skilled reader, in the same vein as the skilled person, did not possess any imagination abilities (referring to case **T 89/00**, Reasons 5), thus they would not consider that both a *functional* separation and different types of *hardware* separation were encompassed by the scope of claim 1.

These arguments fail to convince. First, the board notes that software is executed on hardware, thus in practice a software engineer is well aware of essential aspects of hardware and, similarly, a hardware engineer is well aware of essential aspects of software. Second, the appellant did not explain specifically any alleged differences in interpretation if the skilled reader were defined as a *software* engineer as opposed to a *hardware* engineer, and the board is not aware of any, either. Third, the interpretation of feature (e) of claim 1 is not based on any "imagination", but corresponds to the technically meaningful interpretation of the claim's wording.

2.6 The appellant referred to page 10, lines 26 to 29 of the description as filed and argued that this passage clearly demonstrated that the "memory nodes" were separated from the processors of the system via an "interconnection network".

The board agrees that the "memory nodes" are connected to the processors via the "interconnection network". However, this teaching discloses, at most and implicitly, a specific functional separation, via the interconnection network. Indeed, the "memory nodes" could be disposed on the same substrate as the processor cores, as correctly stated by the appellant (cf. statement of grounds of appeal, page 5, first full paragraph). Furthermore, this passage does not refer to the "related hardware of the processors".

2.7 The passage on page 11, line 35 to page 12, line 18 discloses the operation of the "processors", the "related hardware" and the "memory nodes" only on a functional level. A specific functional separation is disclosed only by stating that "external memory

references from multiple processors" are received, via the interconnection network, by the "active memory unit".

2.8 The appellant referred to Figures 1, 2 and 4 of the application in suit and the corresponding passages of the description.

The board notes that Figures 1 and 2 pertain to the description of the relevant background art. Furthermore, no basis is apparent for singling out from the complete teaching of these Figures the aspect of "separation" of the "memory unit" 112 from the "related hardware of the processors" 104 and 106. Figure 4 does not refer to any "related hardware of the processors". The corresponding description section (pages 10 to 12) discloses that the "memory nodes" are connected to the processors via the "interconnection network". However, as explained above, this teaching discloses, at most a specific functional separation.

2.9 In a further line of argument, the appellant referred to **G 1/93** and stated that the wording "is separate with respect to" was a limiting feature without any technical contribution.

This argument is not convincing. First, "is separate with respect to" is in fact broader than the specific functional separation which is originally disclosed (see point 2.6 above). Furthermore, the "technical contribution"-criterion was established only for escaping the so-called Article 123(2) and 123(3) EPC trap - it does not change the application of the "gold

standard" when assessing compliance with Article 123(2) EPC (see e.g. Reasons 4.3 of **G 2/10**).

2.10 The appellant argued that the skilled person was not concerned with the specifics of the hardware implementation as long as there was at least a functional separation.

However, claim 1 unambiguously refers to the terms "physically" and "hardware", i.e. to hardware specifics (cf. features (c) and (e)).

2.11 Pages 8 and 13 cannot form a basis for deriving feature (e), either. Page 8 does not refer to any "related hardware of the processors" and page 13 (lines 9 to 19) discloses, at most, a specific functional separation.

2.12 Similar observations apply to feature (e1) of claim 1 of the first auxiliary request.

2.13 For these reasons, claim 1 does not comply with Article 123(2) EPC. Thus, the main request and the first auxiliary request are not allowable.

**3. Second auxiliary request - claim 1 - Article 123(2) EPC**

3.1 Feature (b) of claim 1 of the main request was modified in the second auxiliary request as follows:

(b2) a plurality of processors, step caches, and scratchpads;

feature (e) was deleted;

and feature (i) was modified as follows:

(i2) an active memory unit at least functionally connected to a plurality of processors, said step caches, and said scratchpads via said interconnection network.

3.2 The board holds that **features (b2) and (i2)** introduce added subject-matter. In particular, the application as filed consistently discloses that the "step caches" and the "scratchpads" are "related hardware" of the "processors" (cf. page 12, lines 4 and 5, page 13, lines 17 to 19 and page 14, lines 2 to 4 of the description as filed). No basis is present for the "step caches" and the "scratchpads" being independent components of the "system", as presently claimed (cf. the list "a plurality of processors, step caches, and scratchpads" in feature (b2)).

3.3 Furthermore, the application as filed does not disclose that the "step caches" and the "scratchpads" themselves are connected to the "active memory unit" via the "interconnection network" (i.e. **feature (i2)**). The teaching of page 13, lines 9 to 19 merely relates to the transfer of results via the interconnection network. Page 14, lines 2 to 4 does not refer to any "interconnection network".

3.4 The appellant also referred to the principle of prohibition of *reformatio in peius*.

The board notes that this prohibition applies to the legal effect of a decision (in the present case: that the patent application was refused), not to the specific reasons therefor (non-compliance with

Article 56 EPC vs. Article 123(2) EPC). The principle of prohibition of *reformatio in peius* can only apply to appeals against decisions of the opposition division only, i.e. to *inter partes* appeal cases with a sole appellant.

3.5 For these reasons, claim 1 does not comply with Article 123(2) EPC. Thus, the second auxiliary request is not allowable.

**4. Third auxiliary request - claim 1 - admittance**

4.1 Claim 1 of the third auxiliary request was modified in feature (b) as follows:

(b3) a plurality of processors and processor-associated hardware including step caches, scratchpads, and buffers,

feature (d) was modified as follows:

(d3) an interconnection network connecting the plurality of processors and processor-associated hardware, and said multiple data memory nodes for use in ESM architectures,

feature (h) was modified as follows:

(h3) a multi-port cache ~~for~~ connected to the data memory module, said cache being provided with at least one read port and at least one write port, said multi-port cache being configured to hold recently and/or frequently used data stored in the data memory,

feature (i) was modified as follows:

(i3) an active memory unit at least functionally connected to the plurality of processors and processor-associated hardware, via said interconnection network,

feature (j) was modified as follows:

(j3) said active memory unit being connected and configured to operate the multi-part cache upon receiving, via said interconnection network, a multi-operation reference incorporating a memory reference to the data memory of the data memory module from a number of processors of said plurality,

feature (k) was modified as follows:

(k3) wherein responsive to the receipt of the multi operation reference the active memory unit is configured to process the multi-operation reference according to the type of the multi operation indicated in the multi-operation reference and execute inter-processor portion of the multi-operation, utilising cached data in the multi-port cache in accordance with the memory reference and data provided in the multi-operation reference,

and the following feature was added to claim 1:

(l) the data memory node is configured to return the outcome of the executed multi-operation to said

number of processors via said interconnection network.

4.2 This auxiliary request was filed for the first time with the statement of grounds of appeal. Accordingly, it is to be regarded as an "amendment" of the appellant's case within the meaning of Article 12(4) RPBA.

4.3 The appellant did not submit any reasons for submitting the third auxiliary request only in the appeal proceedings (as required by Article 12(4), third sentence, RPBA). It merely stated that "the applicant believes that even in the manner which the Examining Division interpreted the claims of the Second Auxiliary request, the Third Auxiliary request is allowable".

4.4 The second auxiliary request was filed in the course of the first-instance oral proceedings. It was then discussed in detail (cf. minutes, points 5.5 to 5.19) whether the subject-matter of claim 1 involves an inventive step. Thereafter, upon being asked by the chair of the examining division, the appellant refrained from presenting further arguments or submissions (cf. minutes, point 5.20).

4.5 It is apparent from the file that the appellant had an opportunity to file an amended claim request before the examining division, and should have done so, if it wanted to have such claimed subject-matter examined. However, it chose not to do so. Instead, on appeal, the appellant submitted the third auxiliary request which includes numerous amendments and features from the description. This amounts to a "fresh case" on appeal.

4.6 The board first recalls that the appeal proceedings do not form a continuation of the first-instance proceedings. Rather, the primary object of the appeal proceedings is to review the decision under appeal in a judicial manner (Article 12(2) RPBA).

4.7 Furthermore, Article 12(6), second sentence, RPBA, which as a rule prevents admittance of requests that should have been filed in the first-instance proceedings, effectively expresses and codifies the principle that each party should submit all arguments and requests that appear relevant as early as possible so as to ensure a fair, speedy and efficient procedure. An appellant is not at liberty to bring about the shifting of its case to the appeal proceedings as it pleases, with the intention to compel the board either to give a first ruling on the critical issues or to remit the case to the examining division. Conceding such freedom to an appellant, with the intended consequence of shifting the case from the examining division to a new case before the boards of appeal, would run counter to orderly and efficient appeal proceedings. In effect, allowing such an approach would lead to a kind of "forum shopping" which would jeopardise the proper distribution of functions between the departments of first instance and the Boards of Appeal and would not be in line with procedural economy generally (Article 12(4), fifth sentence, RPBA).

4.8 For these reasons, the third auxiliary request was not admitted into the appeal proceedings (Article 12(4), fifth sentence, and 12(6), second sentence, RPBA).

## 5. Fourth and fifth auxiliary requests - claim 1 - admittance

5.1 Feature (e) of claim 1 of the main request was modified in the **fourth auxiliary request** as follows:

(e4) each one of the data memory nodes is functionally separate with respect to related hardware of the processors.

5.2 Features (b2) and (i2) of claim 1 of the second auxiliary requests was modified in the **fifth auxiliary request** as follows:

(b5) a plurality of processors, each associated with step caches and scratchpads;

(i5) an active memory unit at least functionally connected to the plurality of processors, including their associated step caches and scratchpads via said interconnection network.

5.3 The fourth and fifth auxiliary requests were submitted at the oral proceedings before the board. They amount to an amendment to the appellant's appeal case which shall, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the appellant (Article 13(2) RPBA).

5.4 With regard to "exceptional circumstances", the appellant argued that detailed arguments regarding feature (e) had not been provided by the examining division in the decision under appeal, but were only provided by the board in its communication under

Article 15(1) RPBA. Furthermore, the objection under Article 123(2) EPC regarding features (b2) and (i2) was raised for the first time in the board's communication.

The board holds that these are no "exceptional circumstances". It is indeed very common that a board confirms an objection raised in the impugned decision and elaborates further on the reasons. Furthermore, the appellant submitted the fourth and the fifth auxiliary requests only at the oral proceedings before the board while being aware of the board's arguments. In addition, the appellant provided arguments in writing well in advance of the oral proceedings, addressing the board's preliminary opinion issued in relation to the main request, the first and the second auxiliary request. The appellant chose to not file auxiliary requests with this letter but only at oral proceedings. That a board raises a new objection in its communication does not give a party a *carte blanche* to submit amended claims at the latest point in time, i.e. at the oral proceedings before the board (see e.g. also catchwords of **T 2271/18** and **T 2632/18**).

5.5 Furthermore, as explained above with regard to the main request, the application as filed discloses a specific functional separation, via the interconnection network. Hence, feature (e4) as amended does not, *prima facie*, overcome the objections raised by the board (see the criterion of Article 13(1), last sentence, RPBA).

5.6 Similarly, **feature (i5)** does not, *prima facie*, overcome the objection raised by the board with regard to feature (i2) (Article 13(1), last sentence, RPBA). Indeed, feature (i5) still requires that the "step caches and scratchpads" are connected to the "active

memory unit" via the "interconnection network", for which no basis is apparent (cf. point 3.3 above).

5.7 For these reasons, the fourth and fifth auxiliary requests were not admitted into the appeal proceedings (Article 13(2) RPBA).

## Order

## For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

B. Brückner K. Bengi-Akyürek

Decision electronically authenticated